REMARKS

Filed concurrently herewith is a Petition Under 37 CFR §1.181 that the Examiner provide a complete response to the arguments previously of record (e.g., in the Preliminary Amendment filed on September 17, 2003, and clearly ignored in preparation of the rejection currently of record. The essence of these arguments are repeated in the discussion below of the prior art rejections. Applicant has requested in that petition that, since the Office Action mailed August 12, 2005, clearly fails to recognize these arguments, the next Office Action not be made final, since Applicant has not had a chance to adjust claims to any response of these arguments.

It is noted that, notwithstanding any claim amendments made herein, Applicant's intent is to encompass equivalents of all claim elements, even if amended herein or later during prosecution.

Claims 1-16 and 34-37 are all of the claims pending in the present Application. New claims 34-37 have been added. Claim 9 is withdrawn from consideration until an allowable linking claim permits rejoinder.

The Examiner objects to specification because of the characterization in the Preliminary Amendment that this Application is a divisional of parent Application 09/759,101, now U.S. Patent 6,653,240. The Examiner notes that the present Application is not due to a restriction requirement and, therefore, considers that this Application cannot be considered a divisional application. The Examiner also alleges that the claimed invention of the present Application is not distinct or independent from the invention defined by the claims of the parent Application.

In response, Applicant revises the priority statement in the specification to refer to a continuation application rather than a divisional application and respectfully requests that the Examiner reconsider and withdraw this objection.

However, Applicant respectfully traverses the Examiner's characterization that the claimed invention of the present Application is not distinct from that of the parent Application. Distinctness would be inherent upon allowance of the claims of the present Application over the prior art of record, since the Examiner relies upon the same prior art in

both the parent Applicatin and this continuation Application. This issue of distinctness is further discussed in the Applicant's response to the double patenting rejection.

Claims 1-16 stand rejected under the judicially-created doctrine of obviousness-type double patenting as being unpatentable over corresponding claims in the parent Application 09/759,101, now U.S. Patent 6,653,240.

Claims 1,3-6, 10, and 12-16 stand rejected under 35 USC §103(a) as unpatentable over US Patent 6,165,695 5 to Yang et al., further in view of US Patent 6,200,888 to Ito et al. Claims 2, 8, and 11 stand rejected under 35 USC §103(a) as unpatentable over Yang/Ito, further in view of US Patent 6,225,626 to Talbot et al., and claim 7 stands rejected under 35 USC §103(a) as unpatentable over Yang/Ito, further in view of US Patent 6,383,907 to Hasegawa et al.

These rejections are respectfully traversed in view of the following discussion.

I. THE CLAIMED INVENTION

As described and claimed, for example, in claim 1, the present invention is directed to a method for circuit modification of a microelectronic chip comprising at least one conductor in an organic dielectric, in a manner so that a conductive residue from said ion-milling process does not contaminate said organic dielectric.

A protective inorganic surface layer is applied on the organic dielectric. A window is formed in the protective inorganic surface layer to selectively expose an underlying portion of the organic dielectric, the window being located over an area that covers a conductor to be modified by the ion-milling process. The organic dielectric is etched through the window to selectively remove a portion of the organic dielectric adjacent to the conductor.

The ion-milling process is performed on the conductor either to remove conductive material from the conductor to open up an existing routing in the circuit or to add conductive material to the conductor to form a new routing within the circuit.

As explained beginning at line 14 on page 1 of the specification, there is no conventional method that allows ion-milling to be used to modify circuits embedded in organic dielectric layer, since there is no known method that precludes the contamination of

the organic dielectric layer during the ion-milling process. Without such method, as explained at lines 2-3 of page 2, ion-milling inherently utilizes charged ions that impregnate the organic dielectric to defeat electrical isolation.

In contrast, the present invention teaches that the organic dielectric layer be first selectively etched away from the conductor to be modified, so that the conductive residue from the ion-milling does not settle on the organic dielectric material adjacent to the operation. If necessary, the conductive residue from ion-milling process can specifically be also carried away by a passivation gas, such as xenon diflouride, introduced as part of the ion-milling procedure.

II. THE REJECTION BASED ON DOUBLE PATENTING

Claims 1-16 stand rejected under the judicially-created doctrine of obviousness-type double patenting over the claims of the parent Application. Applicant respectfully traverses this rejection.

The Examiner alleges that: "*Although the conflicting claims are not identical, they are not patentably distinct from each other because the claim in the US Patents* (sic) *6,653,240 is narrower by further specifying a second conductor layer.*"

Applicant respectfully disagrees with the Examiner that the claims of the present invention are indistinct from those of the parent application, since the independent claims herein do not require that the ion-milling operation be done on a second, underlying conductor to distinguish from the prior art of record. The improper modification of Yang with Ito was explained in the Preliminary Amendment filed on September 17, 2003, and is repeated hereinbelow in the discussion concerning the prior art rejections.

It is further noted that the claims herein further describe the meaning of the modification to be done by the ion-milling process, thereby clearly adding a distinguishing limitation from the invention defined in the parent Application. It is noted that the Examiner considered the claims allowable in the parent in view of the procedure defined in Yang, which procedure is clearly different from the definition in the claims of the present Application, thereby clearly demonstrating distinctness of the present claims.

It is further noted that, as a matter of law, in order to establish a *prima facie* obviousness rejection, the Examiner has the initial burden of presenting a prior art argumetn in the rejection itself that demonstrates that the claims of the present Application would be obvious over the claims of the parent Application that are directed to an underlying conductor. In the rejection currently of record, the Examiner merely makes a conclusory statement and does not meet his initial burden.

Finally, it is further noted that Applicant declines to submit a terminal disclaimer, since Applicant is clearly entitled to a term adjustment due to the nearly two-year period during which the USPTO did not take up prosecution of this continuation, even though the parent Application passed to allowance in November 2003. A terminal disclaimer would expressly defeat the intent of the term adjustment.

In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw this double patenting rejection.

III. THE PRIOR ART REJECTIONS

The Examiner alleges that Yang, when modified by Ito, renders obvious claims 1, 3-6, 10, and 12-16, when further modified by Talbot, renders obvious claims 2, 8, and 11, and when further modified by Hasegawa, renders obvious claim 7.

Applicant respectfully disagrees and notes again that the Examiner's most recent rejection contained in the Office Action dated August 12, 2005, indicates that Applicant's argument in the Preliminary Amendment for the present Applicant, as initially submitted in the Amendment under 37 CFR §1.116, filed on May 23, 2003, for parent Application, S/N 09/759,101, has never been considered by the Examiner, either in evaluation of the present Application or evaluation of the parent Application.

In the current rejection, essential identical to the final rejection in the parent Application, the Examiner concedes that Yang fails to teach or suggest an ion-milling procedure be done on an underlying conductive ARC layer 62. To overcome this deficiency, the Examiner relies on Ito and alleges that it would have been obvious to one of ordinary skill

in the art to modify Yang to incorporate an ion-milling procedure, as taught in Ito, "... because it will help to remove the naturally oxidized film on the conductive layer."

There are at least three problems with the rejection currently of record.

First, one of ordinary skill in the art would readily recognize that Ito is taken out of context relative to Yang. That is, Ito specifically addresses a manufacturing sequence in which a metal conductor 12 (see Figure 1A) is intentionally left exposed by via 26 for subsequent wire bonding, thereby allowing a natural oxide film to develop on the surface of conductor 12 (column 1 at lines 46-56).

In contrast, Yang does not share this problem identified in Ito. That is, in Yang, the ARC layer 62 is covered by organic dielectric 66 and, therefore, is exposed only during the controlled conditions of the formation of via 140. Thus, if an oxide layer were to be undesirable during this formation, one of ordinary skill in the art would simply provide the environment so that such oxide would not form. Moreover, since ARC layer 62 covers the underlying conductor 60, there would be no oxide layer to form on the upper surface of conductor 60 (see figures 13 and 14). Indeed, at lines 45-50 of column 6, Yang expressly teaches that there is no need to expose the conductor 60 in order to make electrical contact thereto. Therefore, there is no oxide layer on conductor 60 in Yang that requires an ion-milling process to eliminate and there is no reason to suspect that one of ordinary skill in the art would permit formation of an oxide during fabrication of the via 140..

Second, Yang can only be reasonably described as actually teaching against the combination urged by the Examiner in that, according to lines 42-58 of column 9, an RIE is preferably used to etch the organic dielectric layer 66. In lines 51-54 of column 6, Yang expressly teaches that the ARC layer 62 serves to protect the underlying metal 60 during the dielectric etch. The Examiner cannot simply ignore the express contrary teaching of the primary reference itself. (see, e.g., MPEP 2143.01: "Where the teachings of two or more prior art references conflict, the examiner must weigh the power of each reference to suggest solutions to one of ordinary skill in the art, considering the degree to which one reference might accurately discredit another." "The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination." "If proposed modification would render the prior art

invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification." "If the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious.")

Third, even if Ito were to be combined with Yang, the result would still fail to teach the present invention. That is, the ion-milling procedure in Ito is done only to the oxide layer F formed on the top of the surface of conductor 12. There is no suggestion whatsoever in Ito to perform an ion-milling procedure on the conductor itself. Removal of a surface oxide layer by an RIE procedure does not cause the contamination of the dielectric that occurs if the metal itself undergoes an ion-milling procedure. Therefore, neither Yang nor Ito addresses the problem addressed by the present invention.

In contrast to both Yang and Ito, the present invention teaches that an ion-milling procedure that, for example, cuts through the conductor adjacent to an organic dielectric or adds metal to the conductor to form a new circuit, can be done if the dielectric material directly adjacent to the conductor to be modified is first removed in the immediate locality, in order to preclude contamination during the ion-milling procedure. Neither Ito nor Yang teaches, suggests, or even hints at this procedure of first removing adjacent dielectric material prior to conducting the ion-milling modification to the conductor.

The rejection of record introduces Hasegawa to demonstrate that nitride is known in the art as a masking layer and introduces Talbot to demonstrate details of FIB milling. Even assuming, *arguendo*, the Examiner's allegations for these two references, neither of them overcomes the deficiency identified above for Yang and Ito.

A key aspect of the present invention is that it provides a method that allows a conductor at least partially embedded in an organic dielectric layer to be modified by an ion-milling process. No method is known currently that allows reworking by ion-milling of metal conductors embedded in organic dielectric material. Such ion-milling is well known in the art to causing the problem that ions become implanted in the organic material in the area of the ion-milling operation, thereby potentially causing shorts for conductive regions located in the area of the repair.

The present invention solves this problem by removing the organic dielectric adjacent to the conductor to be modified prior to the ion-milling step. After the ion-milling is complete, the volume occupied by the removed organic dielectric material is filled in with a dielectric, typically SiO_2. The present invention provides the advantage that faults or design errors can now be modified for chips having metal conductors embedded in an organic dielectric layer, either during fabrication or even after the chip has been completed.

Part of the Examiner's problem in using Yang as the primary reference in the prior art evaluation is that the process of that reference (e.g., constructing a via using simple etching of the overlying layer and a metal deposition process) does not in any way involve ion-milling of a conductor. Therefore, the problem of ion-milling contamination of the overlying organic layer 66 is not even a problem in Yang. Moreover, since the purpose of Yang is the construction of a via through this layer 66, any contamination of the surface of the overlying layer 66 that contacts the via structure is completely irrelevant since the via itself is conductive and any contamination of the layer 66 in that area would only assist in the conductivity of that via, should the Examiner be able to dream up some ion-milling procedure to be incorporated in fabricating this via.

Therefore, Yang cannot be reasonably described as attempting to address a circuit modification, in the sense of the present invention, since it deals merely with the initial fabrication stage of the device in which a via is being formed. This initial fabrication is an entirely different concept from that of modifying a circuit to either disconnect a conductor already formed, in order to form an open circuit in the conductor, and/or modifying the circuit by adding a new conductor route to connect to another point in the circuit.

That is, in the exemplary embodiments described in the specification, the present invention addresses the problem of correcting a circuit interconnection, either after manufacture or at a stage during fabrication in which one or more conductors have to be modified for a new circuit interconnection. Yang is not attempting to address a modification of a circuit, but, rather, merely explains a technique of forming a via during fabrication of the original circuit, and one that does not even involve ion-milling.

Moreover, Applicant submits that Ito also fails to address the modification of a circuit, in the manner that a modification is described in the present Application. Rather,

similar to Yang, Ito describes a specific initial fabrication steps of the device, an entirely different concept from a circuit modification.

Hence, turning to the clear language of the claims, in Yang there is no teaching or suggestion of: "A method for circuit modification of a microelectronic chip comprising at least one conductor in an organic dielectric, in a manner so that a conductive residue from said ion-milling process does not contaminate said organic dielectric, said method comprising: applying a protective inorganic surface layer on said organic dielectric; forming a window in said protective inorganic surface layer to selectively expose an underlying portion of said organic dielectric, said window located over an area that covers a conductor to be modified by said ion-milling process; etching said organic dielectric through said window to selectively remove a portion of said organic dielectric adjacent to said conductor; and performing said ion-milling process on said conductor to at least one of remove conductive material from said conductor to open up an existing routing in said circuit and add conductive material to said conductor to form a new routing within said circuit", as required by independent claim 1. Independent claims 12 and 14 have similar language.

For the reasons stated above, the claimed invention is fully patentable over the cited references.

Moreover, relative to various other points in the rejection currently of record, Applicant submits the following:

Relative to the urged combination of Yang and Ito, Applicant submits that these two references are non-analogous and, therefore, not properly combinable for an obviousness evaluation. That is, they are respectively placed in different classifications by the USPTO and respectively address different problems from each other and from the problem addressed by the present invention.

Relative to the rejection for claims 3 and 15 on page 5 of the Office Action, Applicant traverses the Examiner's statement that metals can be freely interchanged in the semiconductor environment. Specifically, Applicant traverses that copper would be acceptable to interchange with aluminum in organic dielectric materials in which copper is known to diffuse into the material.

Relative to the rejection for claim 12, Applicant respectfully traverses that the present invention is confined to scenarios in which the conductor is completely embedded, as evidenced by new claim 35. The present invention is applicable in scenarios in which at least one surface of a conductor to be modified is adjacent to an organic dielectric such that ion-milling of that conductor would cause contamination of the organic dielectric material. By selectively etching whatever organic dielectric material is adjacent to the area of the conductor that will receive the ion-milling procedure, the space voided by this etching will not be subject to the ion-milling contamination that has plagued the art.

As is well known in the art, the conductor to be modified might be completely embedded by organic dielectric, but also might be in contact with the organic dielectric only on one or both sides, with top and bottom of the conductor being in contact with some other insulative layer. Applicant intends that such scenarios in which a conductor to be modified is not fully embedded by the organic dielectric is also covered by the claimed invention.

Relative to the rejection for claim 16, Applicant submits that the protective organic layer 70 in Yang is disqualified, since this layer is used as a mask only for purpose of forming the via. Applicant further submits that this confusion again demonstrates that Yang teaches the initial fabrication of the device and is not concerned in any way with a modification of the device after one or more layers have been placed on top of the conductor.

In contrast, claim 16 exemplarily addresses scenarios in which the fabrication has either already been completed and one or more layers cover the area to be modified or the fabrication has progressed to several layers above the conductor requiring to be modified. This is an entirely different concept from that of considering a fabrication masking layer as an additional layer.

Relative to the rejection for claims 2, 8, and 11, wherein the Examiner additionally urges to modify Yang with Talbot, Applicant submits that these two references are non-analogous and, therefore, not properly combinable, by reason of their different classifications and addressing different problems from that of the present invention. Moreover, there is no need in Yang for "... a deeper window portion through the active region", as used by the Examiner as a rationale for modification of the primary reference.

Relative to the rejection for claim 7, in which the Examiner attempts to extract concepts out-of-context, Applicant first submits that Hasegawa is also not properly combinable with Yang, since it is non-analogous art and addresses a different problem from that of Yang or the present invention. It is well known in the art that selection of masking material depends upon the underlying layer to be etched and the specific etch technique to be used. As such, contrary to the Examiner's characterization, one of ordinary skill in the art would not simply substitute materials.

IV. FORMAL MATTERS AND CONCLUSION

In view of the foregoing, Applicant submits that claims 1-16 and 34-37, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance, since withdrawn claim 9 would be subject to rejoinder. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview. The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Assignee's Deposit Account No. 09-0458.

Respectfully Submitted,

Date: 11/14/05

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